

METHOD FOR CLOCK CONTROL OF HALF-RAIL DIFFERENTIAL
LOGIC

5

SWEE YEW CHOE

ABSTRACT OF THE DISCLOSURE

10 Clocked half-rail differential logic circuits are
activated by a delayed clock. According to the
invention, when clocked half-rail differential logic
circuits of the invention are cascaded together, a
delayed clock is provided for each clocked half-rail
15 differential logic circuit and each delayed clock is
timed to at least the delay of the previous clocked
half-rail differential logic circuit. Consequently,
according to the invention, a delay time is introduced
to ensure each clocked half-rail differential logic
20 circuit of the invention is switched or "fired" only
after it has received an input from the previous
clocked half-rail differential logic circuit stage.
According to the invention, this is achieved without
the use of complicated control circuitry.

25